WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a semiconductor die having opposed first and second surfaces, a peripheral edge, and a plurality of bond pads disposed on the second surface in close proximity to the peripheral edge;

a plurality of leads positioned along and in spaced relation to the peripheral edge of the semiconductor die, each of the leads having:

a first surface;

a second surface disposed in opposed relation to the first surface; and

a third surface disposed in opposed relation to the second surface and oriented between the first and second surfaces;

a plurality of conductive bumps electrically and mechanically connecting the bond pads of the semiconductor die to the third surfaces of respective ones of the leads; and

an encapsulating portion applied to and at least partially encapsulating the leads, the semiconductor die, and the conductive bumps.

2. The semiconductor package of Claim 1 wherein the first surface of the semiconductor die is exposed within the encapsulating portion.

3. The semiconductor package of Claim 2 wherein the second surface of each of the leads is exposed within the encapsulating portion.

4. The semiconductor package of Claim 3 wherein:

each of the leads further includes a side surface extending between the first and second surfaces thereof; and

the side surface of each of the leads is exposed within the encapsulating portion.

5. The semiconductor package of Claim 1 wherein the

second surface of each of the leads is exposed within the encapsulating portion.

6. The semiconductor package of Claim 5 wherein:

each of the leads further includes a side surface extending between the first and second surfaces thereof; and

the side surface of each of the leads is exposed within the encapsulating portion.

7. The semiconductor package of Claim 1 further comprising a conductive layer disposed on the third surface of each of the leads, the conductive bumps being electrically and mechanically connected to respective ones of the conductive layers.

8. The semiconductor package of Claim 1, further comprising:

a die paddle having a first surface and a second surface disposed in opposed relation to the first surface;

the first surface of the die paddle being bonded to the second surface of the semiconductor die.

9. The semiconductor package of Claim 8 wherein:

the second surface of the die paddle is disposed in substantially co-planar relation to the second surfaces of the leads; and

the second surface of each of the leads and the second surface of the die paddle are exposed within the encapsulating portion.

10. The semiconductor package of Claim 9 wherein the first surface of the semiconductor die is exposed within the encapsulating portion.

11. The semiconductor package of Claim 10 wherein:

each of the leads further comprises a side surface extending between the first and second surfaces thereof; and

the side surface of each of the leads is exposed

within the encapsulating portion.

12. The semiconductor package of Claim 8 wherein:

the die paddle has a die paddle thickness between the first and second surfaces thereof;

each of the leads has a lead thickness between the first and second surfaces thereof; and

the die paddle thickness is substantially equal to the lead thickness.

13. A method for manufacturing a semiconductor package, the method comprising the steps of:

a) providing a semiconductor die having opposed first and second surfaces, a peripheral edge, and a plurality of bond pads disposed on the second surface in close proximity to the peripheral edge;

b) providing a plurality of leads which each include a first surface, a second surface disposed in opposed relation to the first surface, and a third surface disposed in opposed relation to the second surface and oriented between the first and second surfaces;

c) electrically and mechanically connecting the bond pads of the semiconductor die to the third surfaces of respective ones of the leads through the use of conductive bumps; and

d) applying an encapsulant to the leads, the semiconductor die and the conductive bumps to form an encapsulating portion which at least partially encapsulates the leads, the semiconductor die and the conductive bumps.

14. The method of Claim 13 wherein step (a) comprises:

1) providing a wafer having a plurality of semiconductor dies connected to each other via scribing lines; and

2) separating semiconductor dies from the wafer

by sawing the wafer along the scribing lines.

15. The method of Claim 14 wherein step (1) further comprises fusing the conductive bumps to the bond pads of each of the semiconductor dies of the wafer.

16. The method of Claim 13 wherein step (a) comprises fusing the conductive bumps to respective ones of the bond pads of the semiconductor die.

17. The method of Claim 13 wherein:

step (b) comprises plating a conductive layer onto the third surface of each of the leads; and

step (c) comprises electrically and mechanically connecting the conductive bumps to respective ones of the conductive layers.

18. The method of Claim 13 wherein step (b) comprises providing a die paddle having opposed first and second surfaces and a peripheral edge, and positioning the leads about the peripheral edge of the die paddle in spaced relation thereto.

19. The method of Claim 18 wherein step (c) comprises bonding the second surface of the semiconductor die to the first surface of the die paddle.

20. The method of Claim 13 wherein step (d) comprises forming the encapsulating portion such that the second surface of each of the leads is exposed therein.

21. The method of Claim 13 wherein step (d) comprises forming the encapsulating portion such that the first surface of the semiconductor die is exposed therein.

22. The method of Claim 21 wherein step (d) comprises forming the encapsulating portion such that the second surface of each of the leads is exposed therein.

23. The method of Claim 18 wherein step (d) comprises forming the encapsulating portion such that the second surface of the die paddle is exposed therein.

24. The method of Claim 23 wherein step (d) comprises forming the encapsulating portion such that the first

surface of the semiconductor die and the second surface of each of the leads are exposed therein.